



A short introduction

May 2009

Rapid development of reliable embedded systems

**TTE** Systems

## Overview of this presentation

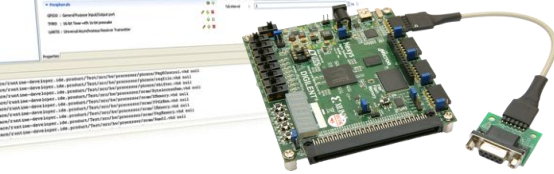
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- At TTE Systems, we develop the RapidITTy™ family of software development tools.
- Based on Time-Triggered (TT) technology, RapidITTy™ tools simplify, automate and accelerate the development of embedded systems that are both reliable and resource efficient.
- RapidITTy™ tools target microcontrollers (MCUs), field-programmable gate arrays (FPGAs) and 'PC' (x86) hardware.
- **This presentation provides an overview of RapidITTy™ FPGA**
- Other members of the RapidITTy™ family provide similar facilities, for microcontroller and x86 targets.

## RapidiTTY™ FPGA: Overview [1]



- Detailed timing analysis
- Integrated compiler & debugger
- Integrated RTOS (royalty free)
- Time-triggered technology



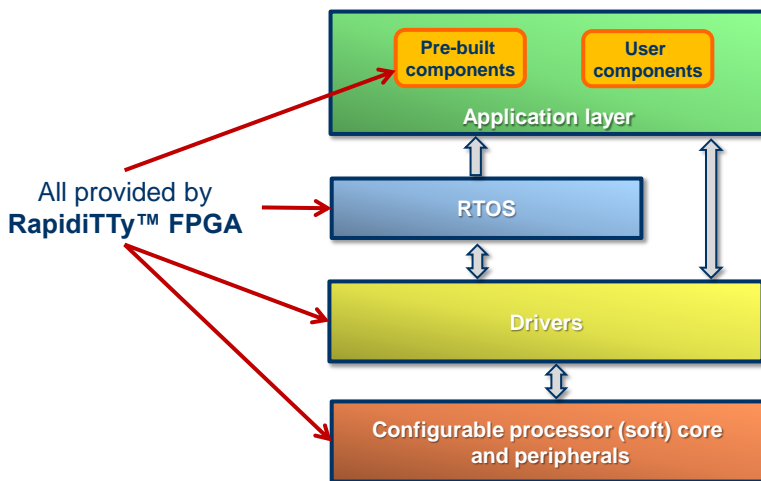
Using the **TTE Processor Builder™** engine and the **PH Processor Toolkit**, you can create a processor which matches your **precise** requirements, with just a few clicks of a mouse (and without writing **any** VHDL code).

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## RapidiTTY™ FPGA: Overview [2]



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## RapidiTTY™ FPGA: Processor toolkits (Overview)

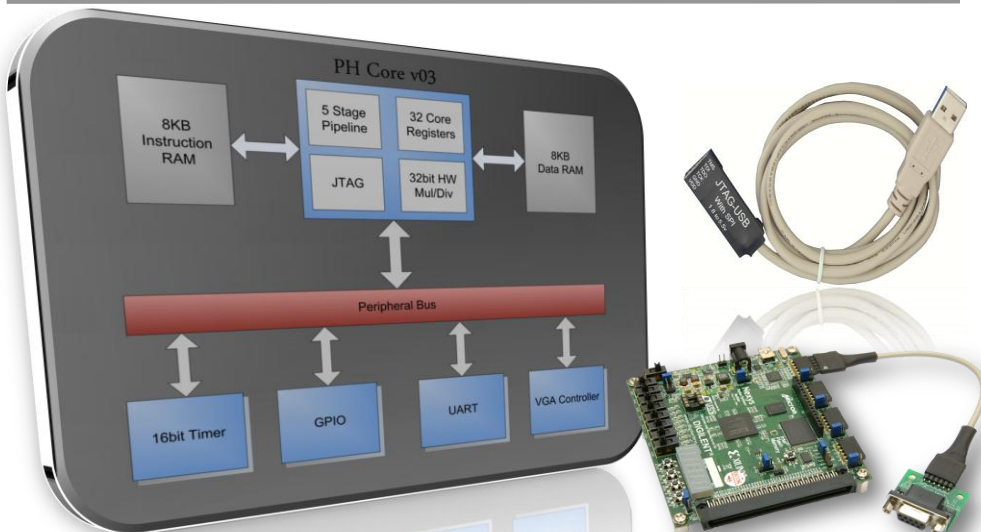
- RapidiTTY™ FPGA ships with Processor Toolkit for the PH processor (with a development licence)
- Processor toolkits provide a highly-configurable platform for the creation of a wide range of reliable embedded systems.
- Processor toolkits offer the following key benefits:
  - Flexible processor configuration during product development by means of the RapidiTTY™ FPGA tool chain;
  - Full programming support from the RapidiTTY FPGA tool chain as your hardware configuration evolves, helping to maximise the speed of your development process and ensuring that your hardware design and software design remain fully synchronised;
  - Highly-predictable behaviour from the completed design (released in FPGA or ASIC form), leading to reduced testing and maintenance costs and higher levels of customer satisfaction.

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## RapidiTTY™ FPGA: Processor toolkits (Example)



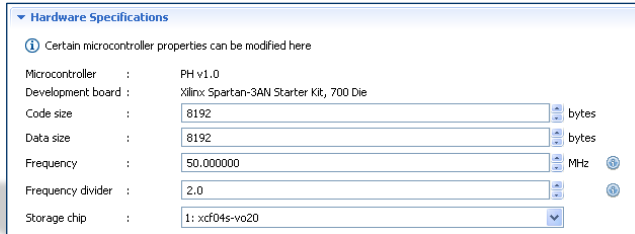
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## RapidiTTY™ FPGA: PH processor [1]

- Using the TTE Processor Builder™ engine, you can configure your PH processor to match your precise requirements
- This takes just a few clicks of a mouse (and you don't need to write any VHDL code)



RapidiTTY™ FPGA also includes full (VHDL) source code for the PH 03 processor core (allowing experienced developers to have full control over their designs).

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## RapidiTTY™ FPGA: PH processor [2]

- Peripherals**  
GPIO0 : General Purpose Input/Output port  
TMRO : 16-bit Timer with 16-bit prescaler  
UART0 : Universal Asynchronous Receiver Transmitter
- Properties for UART0**  
Receive buffer size (bytes) : 50  
Transmit buffer size (bytes) : 50
- Development Board**  
Development board: Nature development board: Xilinx: Spartan-3AN Starter Kit, 700 Die  
CLOCK0 frequency: 50.000000 MHz  
Chips: XCF04S-V020, XCF04S-V020  
Peripheral list:

| Peripheral                   | Pin loc | IO standard | Slew | Drive (mA) | Termination |
|------------------------------|---------|-------------|------|------------|-------------|
| Slide Switch (SLIDE_SWITCH0) | U10     |             |      |            |             |
| Slide Switch (SLIDE_SWITCH1) | U8      |             |      |            |             |
| Slide Switch (SLIDE_SWITCH2) | T9      |             |      |            |             |
| Push Button (PUSH_BUTTON0)   | T14     |             |      |            |             |
| Push Button (PUSH_BUTTON1)   | T16     |             |      |            |             |
| Push Button (PUSH_BUTTON2)   | T15     |             |      |            |             |
| Push Button (PUSH_BUTTON3)   | U15     |             |      |            |             |
| Push Button (PUSH_BUTTON4)   | R13     |             |      |            |             |
| Push Button (PUSH_BUTTON5)   | T13     |             |      |            |             |
| Push Button (PUSH_BUTTON6)   | R14     |             |      |            |             |
- Hardware Overview**  
A circular diagram showing the system components and their connections. Below the diagram, a text box displays the following information:

```
PH Processor:
- flashing LED
- Elapsed time displayed on:
  - UART (115200 bps)
  - VGA
- can blank the display
  - PH resets time (only for some time)
```

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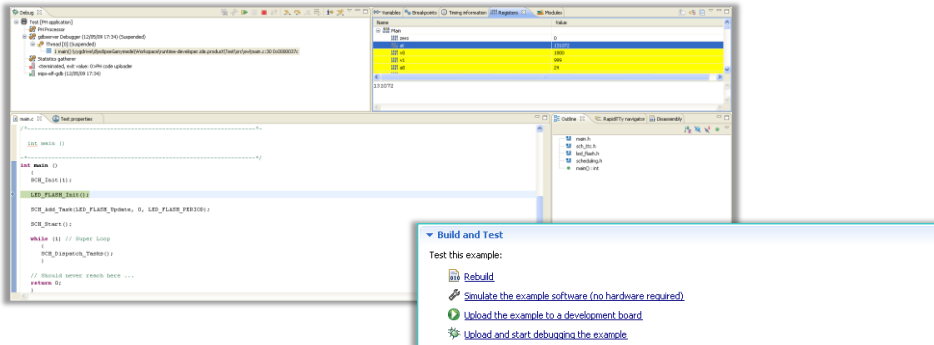
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# RapidiTTY™ FPGA: Debugging

RapidiTTY™ FPGA provides extensive debug support (e.g. breakpoints and single-step from C), fully integrated with the IDE.

The simulator also provides full debug support.



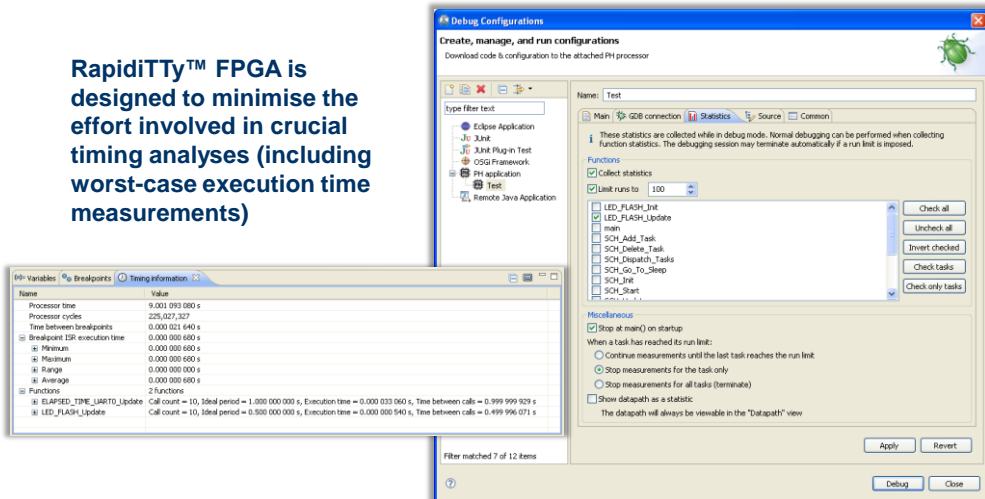
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# RapidiTTY™ FPGA: Timing analysis

RapidiTTY™ FPGA is designed to minimise the effort involved in crucial timing analyses (including worst-case execution time measurements)

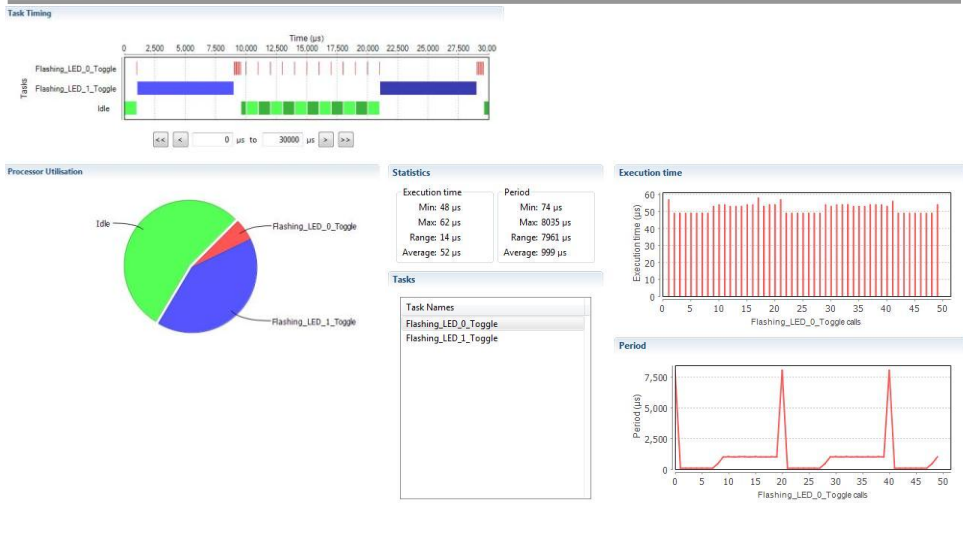


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# RapidiTTY™: Sample timing report

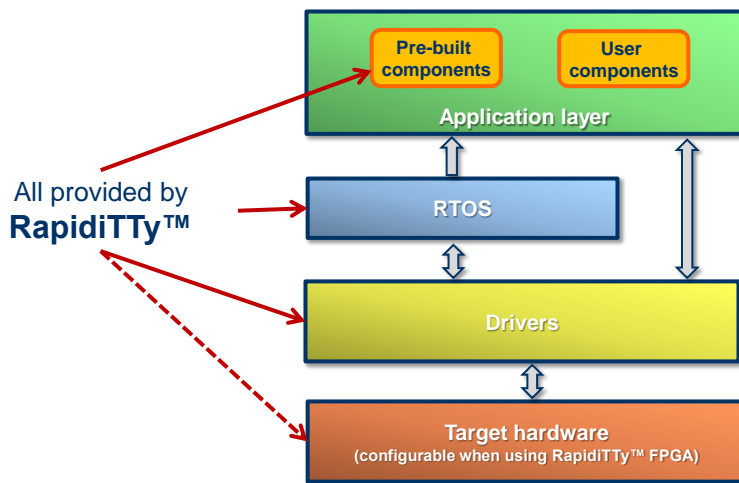


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# RapidiTTY™ family: Overview



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## RapidiTTy™ FPGA: Further information

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- RapidiTTy™ FPGA 2.0 “Getting Started Guide”
- RapidiTTy™ FPGA 2.0 “Tutorial – Getting started”
- RapidiTTy™ FPGA 2.0 “Tutorial – Debugging”
- RapidiTTy™ FPGA 2.0 “Tutorial – Timing Analysis”

- **Available from:**

<http://www.tte-systems.com/downloads/>